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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/851,191	05/08/2001	Samuel D. Pritchett	TI-31005	2844

7590 06/28/2005

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EXAMINER	
PATHAK, SUDHANSHU C	

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 06/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/851,191	PRITCHETT ET AL.	
	Examiner	Art Unit	
	Sudhanshu C. Pathak	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *February 14th, 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *May 8th, 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-to-21 are pending in the application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-5, 7, 9, 12-18 & 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant Admitted Prior Art (AAPA) in view of Troster et al. (An Interpolative Bandpass Converter on a 1.2-um BiCMOS Analog/Digital Array; IEEE Journal of Solid-State Circuits; Vol. 28, No. 4; April 1993; Pages 471-477).

Regarding to Claims 1-5, 7, 9, 12-18 & 20, the Applicant Admitted Prior Art (AAPA) discloses an RF receiver apparatus embodied as an integrated circuit (Fig. 1 & Specification, Page 1, Background of Invention, lines 1-3) comprising a mixing circuitry for mixing an analog RF signal down to an analog IF signal (Specification, Page 3, lines 10-12 & Fig. 1, element 17); an analog IF-to-digital baseband converter, coupled to said mixer for converting said analog IF signal into a digital baseband signal, further comprising an analog-to-digital converter (ADC), a digital IF-to-baseband converter and a matched filter (Fig. 1, elements 12, 14, 15); and an output coupled to said analog IF-to-digital baseband converter for transmitting said digital baseband signal (Fig. 1, element 18). The AAPA further discloses a

baseband processing apparatus (digital signal processor) formed on a second integrated circuit for performing desired digital communications processing coupled to the output of the converter (Fig. 1, elements 13, 16 & Specification, Page 1, Background of Invention, lines 3-6 & Specification, Page 2, lines 1-2). The AAPA also discloses a matched filter (Fig. 1, element 15 & Specification, Page 2, lines 5-13). The AAPA further discloses the matched filter to include a decimator (Specification, Page 2, lines 14-21 & Fig. 2, element 15 & Specification, Page 3, lines 1-18). The AAPA also discloses an example of the digital IF-to-digital baseband converter to include a CORDIC (Coordinate Rotation Digital Computer) circuit (Fig. 2, element 14 & Specification, Page 2, lines 8-13 & Specification, Page 3, lines 1-18). However, the AAPA does not disclose the mixing circuitry and the analog IF-to-digital baseband converter circuitry to be implemented on the same integrated circuit.

Troster discloses a bandpass analog-to-digital (ADC) converter, implemented on a 1.2um BiCMOS Analog/Digital array, for a cellular radio mobile (systems) receiver (Abstract, Page 471, lines 1-8). Troster also discloses implementing the ADC wherein the input is an analog IF frequency signal and is converted to digital baseband signal (Page 472, Fig. 1 & Page 471, Section II, Converter Architecture, Right-hand column –to-Page 473, Section II, Converter Architecture, Left-hand column). Troster also discloses implementing the converter architecture using BiCMOS technology used for the fabrication of the mixed array, which has been optimized for high performance analog/digital (mixed signal) applications and further

optimized for prototyping of interfaces between high frequency analog signals and complex digital baseband signals (Page 473, Section III, BiCMOS Implementation, Right-hand column). Troster also discloses the a BiCMOS technology for a monolithic implementation on a single integrated circuit of mixed signal circuit components for processing high frequency analog signals and digital baseband signals (Page 475, Fig. 6 & Page 473, Section III, BiCMOS Implementation, Right-hand column & Page 475, Left-hand Column, Section "Floorplan" & Page 476, Left-hand column, Section V, Conclusion). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Troster teaches implementing a BiCMOS technology for the implementation of a mixed signal (analog/digital) circuit components and further implementing a bandpass analog IF-to-digital baseband converter and this can be implemented in the receiver as described in the AAPA so as to provide a monolithic integrated signal path from a high frequency signal to a baseband signal so as to provide high level integration desired for cellular mobile transceivers.

4. Claim 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant Admitted Prior Art (AAPA) in view of Troster et al. (An Interpolative Bandpass Converter on a 1.2-um BiCMOS Analog/Digital Array; IEEE Journal of Solid-State Circuits; Vol. 28, No. 4; April 1993; Pages 471-477) in further view of Patel et al. (6,480,528).

Regarding to Claim 6, the AAPA in view of Troster discloses an RF receiver apparatus embodied as an integrated circuit comprising a mixing circuit and an

analog-to-digital baseband converter wherein the converter further comprises a filter as described above. However, the AAPA in view of Troster does not disclose the filter further including a quantizer.

Patel discloses a method and receiver for processing a desired signal wherein the desired signal is sampled, processed by a matched filter and then quantized (Abstract, lines 6-9, Column 2, lines 63-65 & Column 3, lines 39-41, 59-67 & Fig. 4-5). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Patel teaches implementing a quantizer for quantizing the matched filter output and this can be implemented in the RF receiver apparatus as described in the AAPA in view of Troster so as to provide a predetermined number of bits of resolution of the data, thus satisfying the limitation of the claim.

5. Claims 8, 10-11, 19 & 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant Admitted Prior Art (AAPA) in view of Troster et al. (An Interpolative Bandpass Converter on a 1.2-um BiCMOS Analog/Digital Array; IEEE Journal of Solid-State Circuits; Vol. 28, No. 4; April 1993; Pages 471-477) in further view of Fukuda et al. (4,665,532).

Regarding to Claims 8, 10-11, 19 & 21, AAPA in view of Troster discloses a RF receiver apparatus comprising a mixing circuitry, an analog IF-to-digital baseband signal converter and a baseband processing apparatus physically separate from the RF receiver apparatus as described above. However, AAPA in view of Troster does not disclose the analog IF-to-digital baseband converter to include a parallel-

to-serial converter connected between said analog IF-to-digital baseband converter and said output, said parallel-to-serial converter providing serial formatted.

Fukuda discloses a parallel-to-serial converter for converting data in a parallel format (I & Q) into a serial format after demodulation of the received signal so as to recover the transmitted data in the desired (serial) format (Fig. 2, element 210 & Column 3, lines 29-42 & Column 4, lines 20-35). Fukuda further discloses a clock implemented in a parallel-to-serial converter and a serial-to-parallel converter (Fig. 5, element "CLK"). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Fukuda teaches a parallel-to-serial converter, and this can be implemented in the receiver as described in AAPA in view of Troster so as to provide a serial data stream received as transmitted by the transmitter, thus satisfying the limitation of the claim. Furthermore, the conversion of the received serial data, in the baseband apparatus, and converting the data to parallel format is a matter of design choice depending on the application and format of the data transmitted from the transmitter.

Response to Arguments

6. Applicant's arguments with respect to claims 1-to-21 have been considered but are moot in view of the new ground(s) of rejection.

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, it is recommended to the applicant to amend all the claims so as to be patentable over the cited prior art of record. A detailed list of pertinent references is included with this Office Action (See Attached "Notice of References Cited" (PTO-892)).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sudhanshu C. Pathak whose telephone number is (571)-272-3038. The examiner can normally be reached on M-F: 9am-6pm.

    - If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571)-272-3056
    - The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

- Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sudhanshu C. Pathak

STEPHEN CHIN
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